AMENDMENT UNDER 37 C.F.R. § 1.111
APPLICATION NO. 10/058,804
ATTORNEY DOCKET NO. Q68166

REMARKS

Claims 1-8 are all the claims pending in the application. By this Amendment, Applicants add claims 7 and 8. Claim 7 is similar to original claim 6, and claim 8 raises no new matter and is clearly supported on Fig. 2 and the specification at, e.g., pages 5-7. In addition, claims 1-6 have been amended solely for the purpose of improved readability. Since such amendments are made to correct minor, basic elements, Applicants submit that that they do not narrow the scope of the claim and do not raise any Festo implications.

Summary of the Office Action.

Applicants thank the Examiner for initialing the Information Disclosure Statement, Form 1449A and for acknowledging all claims for priority under 35 U.S.C. §119(e), as well as the receipt of the translated priority documents.

However, the Examiner failed to acknowledge that the drawings are accepted. Therefore, Applicants respectfully request the Examiner to check the appropriate box on the Form PTO-326 indicating that the drawings are accepted. Finally, the Examiner has indicated that the specification is objected to for lack of headings and claims 1-6 are rejected under 35 U.S.C. § 112, second paragraph and under 35 U.S.C. § 102(e).

Objection to the Specification.

The Examiner objected to Applicants' specification for lacking headings. Applicants herein amend the specification to include the headings. In view of these amendments to the specification, Applicants respectfully request the Examiner to withdraw this objection.

Rejection under 35 U.S.C. § 112, second paragraph.

The Examiner rejected claims 1-6 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner has only provided reasons for rejecting claim 2 (see page 2-3 of the office action). Specifically, claim 2 is indefinite for reciting "a first switch

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transistor (M3') placed in parallel to the first cascode transistor (M4) and a second switch (M5') placed in parallel to the second cascode transistor (M6)." The Examiner asserts that Fig. 2 does not show these elements being in parallel to one another.

Applicants respectfully disagree. This is clearly supported by the specification as well as shown in Fig. 2. Fig. 2 clearly shows the split of current at the drain nodes A and B. Circuits are parallel when they are connected across the power source instead of having the power source pass through each one in the series.[1] M3' and M4 are not connected in a series and are thus, parallel (because of the split of the current at the nodes A and B). As a result, Applicants respectfully request the Examiner to withdraw this rejection.

Prior Art Rejection.

The Examiner rejected claims 1-6 under 35 U.S.C. § 102(e) as being anticipated by USP 6,415,007 to Kawasumi (hereinafter "Kawasumi"). Applicants respectfully traverse this rejection and respectfully request the Examiner to reconsider this rejection in view of the comments, which follow.

Of these claims, only claim 1 is independent. Claim 1 requires:

> an intermediate switch transistor (M3, M5) is placed between the drain node (A, B) and the cascode transistor (M4, M6).

The Examiner asserts that claim 1 is directed to a PLL charge pump and is anticipated by Kawasumi. The Examiner asserts that Kawasumi's p-channel MOS transistor (P6) and n-channel MOS transistor (N6) is equivalent to intermediate switch transistor (M3, M5) as set forth in claim 1 (see page 4 of the Office Action). Applicants respectfully disagree with the Examiner. Applicants have carefully studied Kawasumi's discussion of the charge pump with MOS transistors, which is not similar to a charge pump with an intermediate switch transistor (M3, M5) as set forth in claim 1.

[1] http://www.homeglossary.com.

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Kawasumi teaches a charge pump with a first and a second sub charge including common charging and discharging terminals and performing charging/discharging operations. The second sub pump performs the opposite of the first sub pump. That is if the first sub pump is charging, the second sub pump is discharging and visa versa (*see* Abstract).

Specifically, Kawasumi teaches a charge pump 18 with two sub charge pumps in PLL 14 (Fig 5; col. 9, lines 6 to 12). Each sub pump has a p-channel MOS transistor (hereinafter "p") p1 connected to a power voltage VDD, and its drain connected to the source of a p2. The drain of p2 is connected to p3, which in turn is connected to a low pass filter (LPF). Also, the drain of p3 is connected to the drain of n-channel MOS transistor (hereinafter "n") n1 and its source is drain of n2, which is connected to the drain of n3 connected to the reference voltage source (Fig. 8; col. 9, lines 5 to 38).

The second sub pump has a voltage power source VDD connected to p5, which drain is connected to p6. Similarly, the drain of p6 is connected to p7 and the drain of p7 is connected to LPF and to the drain of n5, which in its turn is connected to n6, n7 and then reference voltage source. Up signal is used to enable signal at input gate p6 and down signal is used to disable signal at the input of n7 (Fig 8; col. 9, line 48 to col. 10, line 8). Injunction capacitors, C1, C2, C3 and C4 are placed between transistors p1 and p2, n2 and n3, p5 and p6, n6 and n7, respectively (col. 9, lines 28 to 32 and lines 61 to 65). When the charge pump 18 starts charging, the potential drain of p1 becomes operable after the accumulation of electricity in the capacitor C1. When the charge pump 18 starts discharging, the potential drain of p1, the potential drain of n3 becomes operable after the accumulation of electricity in the capacitor C2 (col. 10, line 62 to col. 11, line 19).

However, Kawasumi teaches just a number of p-channel MOS transistors and a number of n-channel MOS transistors, which are field-effect transistor of metal-oxide-semiconductor. Transistors p5, p6 and p7 are equivalent to each other, connected in a series to drain the current. Similarly, transistors n5, n6 and n7 are equivalent to each other, connected in series to enhance the current. That is Kawasumi teaches that all transistors are just MOS and fails to teach or

suggest switch transistor placed between a node and a cascode transistor. In short, Kawasumi teaches only one MOS transistors and fails to teach or suggest a switch transistor.

Therefore, *intermediate switch transistor placed between cascode transistor and a node*, as set forth in claim 1, is not suggested or taught by Kawasumi, which lacks an intermediate switch transistor placed between cascade transistor and a node. For these reasons, Applicants respectfully submit that independent claim 1 is patentably distinguishable from Kawasumi. Applicants therefore respectfully request the Examiner to withdraw this rejection of independent claim 1. Also, Applicants respectfully submit that claims 2-6 are allowable at least by virtue of their dependency on claim 1.

New Claim.

In order to provide more varied protection, claim 8 is added. Applicants respectfully point out that claim 8 recites: *wherein said second intermediate switch transistor is positioned between said node and said second cascode transistor*. This limitation is similar to the limitation of an intermediate switch transistor placed between cascode transistor and a node recited in claim 1. Since claim 8 contains features that are similar to the features argued above with respect to claim 1, those arguments are respectfully submitted to apply with equal force here.

Also, claim 8 recites two intermediate switch transistors being between a node and a corresponding cascode transistor. Kawasumi clearly does not teach or suggest having more than one transistor between a node and a corresponding transistor. Thus, claim 8 patentably distinguishes over Kawasumi.

Conclusion and request for telephone interview.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,

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